Canceled

25. The method of Claim 19 wherein the body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

REMARKS

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached pages are captioned "**Version With Markings to Show Changes Made.**"

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

In re Patent Application of
CROCE ET AL.
Serial No. **Not Yet Assigned**
Filed: **Herewith**

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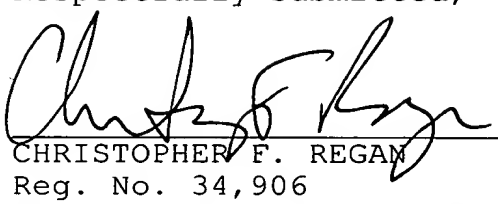
Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at page 2, line 18 has been amended as follows:

A typical shape of the depletion regions of the two above noted junctions is illustrated in FIG. 1a where the source 14, the body region **13**, and the gate are connected to a reference potential GND (i.e., Vg=Vsub=Vs=0) and a certain VDS voltage (e.g., VDS=20V) is applied to the drain. Under these operating conditions, the junctions are inversely biased because of the applied VDS voltage, and the respective depletion regions extend into the drain well region down to a certain depth. By further incrementing the VDS voltage, as shown in FIG. 1b (e.g., VDS=25V where Vg=Vsub=Vs=0), the depletion regions of the junctions between the substrate and the drain well region **12** and between the drain well region and the body region **13** merge. This completely depletes the drain well region **12**, thus producing the desired RESURF condition.

Paragraph beginning at page 4, line 16 has been amended as follows:

FIG. 2a is a cross-sectional view illustrating a traditional LDMOS structure according to the prior art; [and a]

FIG. 2b is a cross-sectional view illustrating an LDMOS structure of the invention;

Paragraph beginning at page 5, line 24 has been amended as follows:

The principles upon which the RESURF LDMOS structure of the invention are based will be better understood with reference to FIGS. 3a and 3b. The BV measurements illustrated in FIG. 3a were obtained with Vds=70V and Vg=Vs=Vsub=0V, and the PT measurements illustrated in FIG. 3b were obtained with Vds=Vg=Vs=70V and Vsub=0V. As shown in FIG. 3b, even if relatively high voltages are applied to the drain and source (typical of a high-side application), the drain well region **12** will be completely depleted of its charge before the body buffer region **15** is depleted. This is due to the heavier doping of the body buffer region **15**. This substantially prevents the occurrence of PT phenomena at relatively low voltages, which in turn enhances the performance of the structure of the invention under critical conditions of use.